## REMARKS/ARGUMENTS

Reconsideration is respectfully requested.

The Abstract has been amended as suggested by the Examiner. Withdrawal of the objection is respectfully requested.

Claims 1-8 are pending in the present application before this amendment. By the present amendment, Claim 2 has been canceled without prejudice, and Claims 1, 3, and 7 have been amended. No new matter has been added.

Claims 1, 3, and 7 stand objected to for containing informalities for use of the word "if". Applicant, however, is not aware of any rules in the U.S. patent law and the MPEP §2173 that consider the word "if" as an improper claim language of indefiniteness. Applicant respectfully finds no authority that prohibits use of the word in a claim, just as the word "when" is not a prohibited claiming language. Nevertheless, the suggested amendments have been made in Claims 1, 3, and 7 to render the present issue moot, and withdrawal of the objection is therefore respectfully requested.

Claims 1-2 rejected under 35 U.S.C. § 102(b) as being anticipated by a Japanese Patent Reference No. JP411068559 (Igura-JP). The "et al." suffix, which may appear after a reference name, is omitted in this paper.

Applicant respectfully notes that the cited Igura-JP reference is in Japanese, and no English translation was provided to the Applicant with the Office Action. Applicant finds very difficult to follow Igura-JP due the non-English disclosure and question whether anyone of ordinary of skill in the pertinent art who is not versed in Japanese can follow and understand the base of rejection stated in the Office Action page 3, Item 5.

Nevertheless, the counterpart U.S. Patent No. 6,066,988 (Igura-US) has been identified and relied on by the Applicant in preparing the present paper responding to the Office Action. A copy of Igura-US is also submitted to the Examiner for reference.

The Office Action cites Igura-JP, FIG. 9 (which is same as Igura-US, FIG. 11) in rejecting the independent Claim 1.

Applicant respectfully notes that a clock divider 50 such as that shown in FIG. 1 (Related Art) is well known by those skilled in the pertinent art. As disclosed in the Specification page 3, lines 8-14, and shown in FIG. 1 (Related Art), the clock divider 50 divides the frequency of the internal clock (the output of the clock buffer 10) and generates a specified reference clock. The specified reference clock is delayed by the dummy delay circuit 60 (having the identical structure of the delay circuit 20) and processed by the replica delay unit 90. The phase comparator 70 (FIG. 1) of the prior art compares the phase or the difference in the time delay between the specified reference signal (i.e., output of the clock buffer 10) and the delayed signal outputted from the replay delay unit 90 as shown in FIG. 1 and described in the Specification page 3, line 24 to page 4, line 6. In a conventional circuit, the comparison of the **phase** as performed by the phase comparator 70 is used to control the delay controller 80 such that the DLL circuit causes the internal clock and the external clock to have the same phase by, for example, compensating the time delay occurred in the internal clock.

However, the conventional delay circuit (an example of which is shown in FIG. 1) has problems in that it cannot perform a normal operation if the period of the external clock input is shorter than the delay time in the replica delay circuit as the related problems are well described in the Specification page 10, line 17 to page 11, line 12 and

FIG. 8.

Among many objectives of the present invention, the presently claimed invention solves the above-mentioned problem of the prior art by utilizing, inter alia, a clock pulse width detector 100 as shown in FIG. 9. The clock pulse width detector 100 "detects" the "pulse width," and this is not same as comparing the phase difference of two given signals performed by the phase comparator 70 of the prior art. That is, as described in the Specification page 17, line 19 to page 18, line 8, the pulse width detector 100 "detects" whether or not the **pulse width** of the input clock signal is longer than the predetermined delay time" (Specification page 18, lines 4-8). An example of the structure and operations of the clock pulse width detector 100 that detects the pulse width of the clock signal in comparison to a predetermined value is described in detail in the Specification page 17, line 11 to page 20, line 11 and shown with respect to FIGS. 11-12. For example, a low level pulse signal is generated at the node b (FIG. 12) when the pulse width of the clock signal exceeds the predetermined delay time, and a high-level pulse is generated when the pulse width of the clock signal less the predetermined delay time (Specification page 17, line 19 to page 18, line 3).

Accordingly, this aspect of the present invention is recited in Claim 1:

> --a **detection unit** for detecting whether a **pulse width** of the **external input clock** is narrower or wider than a **reference set value**--.

The Examiner cites Igura-JP, FIG. 9, element 2, (which is Igura-US, FIG. 11) as being comparable to the claimed --**detection unit** for detecting whether a pulse unit of the external input clock is narrower or wider than a reference set value--. However, the structure shown in Igura is substantially different from the presently claimed invention.

Applicant respectfully points out that the phase comparator 20 (Igura-US, FIG. 11) and the phase comparator 43 (Igura-US, FIG. 1) share the identical structure and the details of the structure and operations are well shown in FIG. 5 described in Igura-US, col. 8, lines 8-62.

Referring to FIG. 5, which shows the structure of the "phase comparator of a pulse width difference detection type" of Igura, the circuit of FIG. 5 is impossible to detect wether a pulse width of the "SCLK" signal is narrower or wider than the "RCLK" signal. That is, the output signal 113 of Igura **cannot** tell or detect whether one input signal is narrower or wider in comparison to the other input signal. Instead, the "phase difference signal" or "U/D" of the output signal 113 (Igura-US, col. 8, lines 31-32) is set to high whenever there is a pulse width difference between the two input signals. To be more specific, the signal 113 will be high whenever either one of "SLCK" and "RCLK" is high but will be low whenever both "SLCK" and "RCLK" are high or low. This aspect of Igura is well described in Igura-US, col. 8, lines 51-55 that the "output signal 113 is set to high or low during the time period which is proportional to the time difference between the pulse width of the RCLK and the pulse width of SCLK." Thus, Igura at best is capable of detecting the pulse width difference of two input signals but does not teach or disclose the claimed **detection unit** that detects --whether a **pulse width** of the external input clock is **narrower or wider** than a reference set value--. Igura can only indicate that there is a difference in pulse width but cannot detect whether the pulse width of one input signal is narrower or wider than another input signal.

At least on this ground, among other reasons, Applicant respectfully submits that the independent Claim 1 is not taught (or suggested) by Igura-JP and/or Igura-US.

Accordingly, withdrawal of the rejections with respect to Claims 1-2 is respectfully requested.

Claims 3-8 are indicated as being allowed if the objections to any of these claims set forth in the Office Action are removed.

With respect to the reasons for allowance set forth in the Office Actoin, page 3, Item 7, pursuant to 37 C.F.R. § 1.104(e), Applicant respectfully disagrees with the Examiner's Statement of Reasons for Allowance, to the extent that the Statement might be construed in any way to limit the scope of the allowed claims.

Applicants generally agree with the Office Action with respect to the reasons for allowable subject matter that the prior art of record fails to teach or fairly suggest the claimed delay locked loop having the specifically recited structures. However, numerous other grounds of allowability are also present, for example, in view of Igura or other cited references since they do not relate to the claimed structure of the detection unit, among others.

For the reasons set forth above, Applicant respectfully submits that Claims 1-8, pending in this application, either has been allowed or are in condition for allowance. This amendment is considered to be responsive to all points raised in the Office Action. Accordingly, Applicant respectfully requests a Notice of Allowance in the next action.

Should the Examiner have any remaining questions or concerns, the Examiner is encouraged to contact the undersigned attorney by telephone to expeditiously resolve such concerns.

Respectfully submitted,

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